A Modulation Method for Reducing DC-link Voltage Ripple in Open-end Winding Motor Drive Systems

Kota Sato [1)] Shinya Yano [1)] Kenta Emori [1)]

1) Nissan Motor Co., Ltd., 1, Natsushima, Yokosuka, Kanagawa 237-8523, Japan

E-mail : kotasato@mail.nissan.co.jp

E-mail : shinya-yano@mail.nissan.co.jp

E-mail : kemori@mail.nissan.co.jp

ABSTRACT: For motor drive systems used for open-end winding motors supplied by a dual-inverter configuration, this study proposes a modulation method that can reduce the DC-link voltage ripple by reducing the second harmonic component of the carrier frequency ($2f_c$ component) of the DC-link current (I_{dc_link}). The proposed method utilizes two triangular carrier waves, one shifted by 90° relative to the other, and selects the carrier wave used for the modulation of each phase according to the phase of the command voltage vector. Simulation results indicate that the proposed method can reduce the $2f_c$ component of I_{dc_link} by 77% compared to that achieved using the sinusoidal pulse-width modulation (SPWM) method, which uses the same carrier wave for all phases, under operating conditions that maximize the DC-link voltage ripple. The reduction effect of the I_{dc_link} is also validated by the experiment, indicating the usefulness of the proposed method.

KEY WORDS: open-end winding motor, DC-link capacitor, DC-link voltage ripple reduction, Pulse-width modulation

1. INTRODUCTION

A propulsion system for electric vehicles (EVs) requires various power ratings depending on the vehicle size [(1)]. Open-end winding motors have been identified as a viable solution for achieving high-power systems [(2)]. Conventionally, in EVs, a star-winding motor is driven using a single inverter. However, in such configurations, it is necessary to increase the power rating of the switching devices within the inverter to accommodate high-power demand of the system. In contrast, an open-end winding motor drive system utilizes two inverters to increase the applied voltage to the motor. Compared to the conventional system, this configuration achieves a higher voltage supply to the motor while maintaining the same battery voltage, thereby eliminating the need to enhance the voltage ratings of the switching devices.

This study aims to enhance the power density of an open-end winding motor drive system with a non-isolated dual inverter by reducing the size of the DC-link capacitor. DC-link capacitors, which mitigate the voltage ripple in DC lines, typically occupy significant volume within inverters [(3)]. The required capacitance to mitigate voltage ripple is mainly determined by harmonic components of the carrier frequency (nf_c components) of the DC-link current (I_{dc_link}). Therefore, the suppression of nf_c components of $I_{dc-link}$ can lead to a reduction in the required capacitance.

This study proposes a modulation method to attenuate the second harmonic component of the carrier frequency ($2f_c$ component) of $I_{dc-link}$, which are the primary contributors to the voltage ripple. In particular, the proposed method utilizes two distinct carrier waveforms with a 90° phase shift relative to each other. These two types of carrier waves are appropriately switched according to the phase of the command voltage vector generated by the current controller, thereby effectively suppressing the $2f_c$ component. Moreover, the results of simulation and experiments conducted in this study are presented to prove the effectiveness of the proposed method.

2. OPEN-END WINDING MOTOR DRIVE SYSTEM

Figure 1 shows an open-end winding motor drive system with a non-isolated dual inverter, in which a DC-link capacitor is inserted into the power line shared by the two inverters to suppress the voltage ripple caused by semiconductor switching.

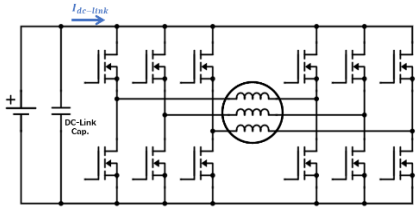


Fig. 1. Open-end winding motor drive system.

The method used in (4) to obtain the I_{dc_link} spectrum during inverter operation by a double Fourier series analysis was utilized to obtain the same for the circuit shown in Fig. 1. The results indicated that, among all carrier frequency components, the $2f_c$ component was the largest when the power factor was 1.0. The $2f_c$ component of the I_{dc_link} versus the modulation rate *M* is shown in Figure 2. The spectrum magnitude was normalized to the armature current norm (I_a). *M* is defined as:

$$M \equiv \sqrt{\frac{2}{3}}\frac{V_a}{V_{dc}} \quad (1)$$

where, V_{dc} is the supply voltage and V_a is the norm of the command voltage vector in the *dq*-plane.

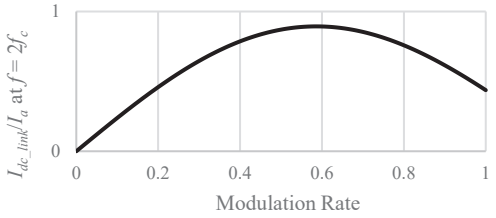


Fig. 2. Change in the $2f_c$ component with respect to the modulation rate.

Figure 2 shows that the $2f_c$ component of I_{dc_link} reaches its peak value when the modulation rate is approximately 0.6. Generally, the armature current reaches its highest value at the maximum torque. Thus, the $2f_c$ component of I_{dc_link} is usually worst at the operating point where torque is maximum and modulation rate is 0.6. The DC-link capacitor must be designed such that the DC-link voltage ripple is suppressed below a specified threshold at the operating point. Therefore, suppressing nf_c components of I_{dc_link} at this point will reduce the required DC-link capacitance. Furthermore, I_{dc_link} spectrum depends not only on the modulation rate but also on the power factor. Therefore, the power factor should also be considered during the detailed design phase.

3. PROPOSED MODULATION METHOD

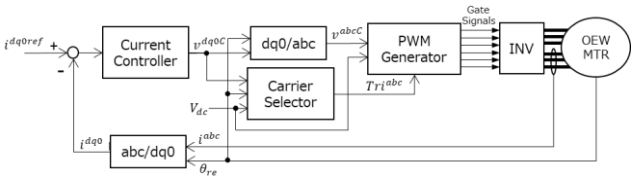


Fig. 3. A schematic of the proposed control system.

Figure 3 shows the proposed control system in which calculates the phase of the command voltage vector in the carrier selector. Moreover, it determines the carrier wave used to modulate each phase according to the preset phase sector to which it belongs. In an open-end winding motor drive employing a non-isolated dual inverter, a zero-sequence current path is formed, exhibiting an impedance lower than that of the *dq*-axis. Therefore, to prevent an unnecessary zero-sequence current flow, the zero-sequence voltage must be controlled. To achieve this, the control system shown in Figure 3 uses a current vector control strategy that adds the zero-sequence to the *dq*-axis. Generally, suppressing zero-sequence current requires controllers with a faster response time than those used for *d*- and *q*-axis currents. Consequently, it is necessary to adopt approaches such as combining feedforward controllers [5], [6] with a feedback controller that exhibits high gain only at specific frequencies [7]. The proposed modulation method requires a controller with a higher gain for zero-sequence current suppression. However, because the objective of this study was to examine the ripple reduction effect of the DC-link voltage, it was assumed that the controller had a sufficiently fast response to suppress the zero-sequence current. The impact of the proposed method on the controller design will be investigated in future.

Figure 4 and Table 1 detail the phase sectors that can be set for the voltage vector space that can be generated by the dual inverters and the carrier selection in each sector. In the example shown in Figure 4, because the voltage command vector V^C belongs to Sector I, pulse-width modulation (PWM) is executed with Tri-1 for Phases *b* and *c*, and with Tri-2 for Phase *a*. This is detailed in Table 1, where Tri-1 denotes the reference carrier wave and Tri-2 is the second carrier wave shifted by 90°.

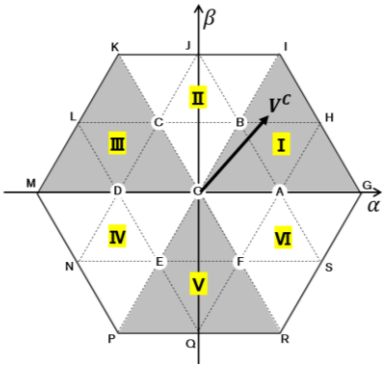


Fig. 4 Space voltage vectors of a dual inverter.

Table 1. Carrier selection based on the phase sector.

Sector	Tri-1	Tri-2
Ⅰ	b,c	a
Ⅱ	a,b	c
Ⅲ	c,a	b
Ⅳ	b,c	a
Ⅴ	a,b	c
Ⅵ	c,a	b

4. SIMULATION

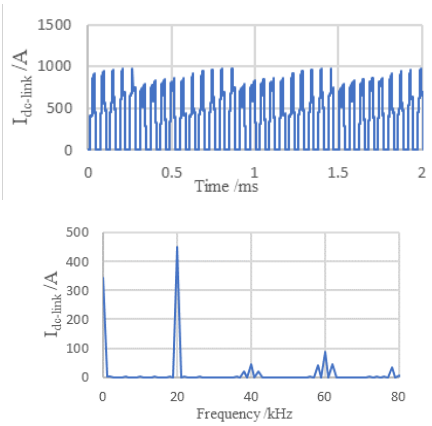
The effect of the proposed modulation method on reducing the $2f_c$ component of I_{dc_link} was verified using the circuit simulator software PLECS (Plexim). The simulation conditions are listed in Table 2.

Table 2. Simulation conditions.

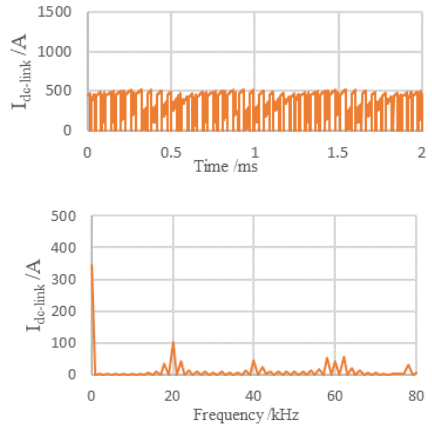
Name	Description	Value	Unit
fc	Carrier Frequency	10	kHz
Vdc	Inverter DC Voltage	400	V
Ia	Armature Current	600	A
cosθ	Power factor	0.87	-
M	Modulation Rate	0.6	-

$I_{dc-link}$ waveforms under the given conditions and the spectrum obtained by Fast Fourier Transform are shown in Figure 5. The conventional modulation approach uses the same carrier wave in all three phases. As shown in Figure 5, the proposed modulation approach reduced the $2f_c$ (20 kHz) component by 77% compared to that of the conventional method (from 448 A to 103 A).

Figure 6 shows the phase current waveforms for each modulation method. The proposed modulation scheme changed the current ripple of the carrier harmonics due to the PWM voltage by dynamically shifting the carrier phase. The detailed impact of the change in the current ripple of the carrier harmonic on the motor will be investigated in future studies.

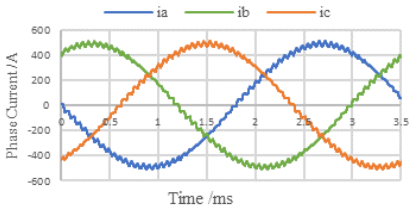


(a)

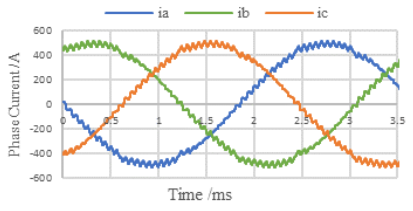


(b)

Fig. 5. Simulation results obtained for I_{dc_link} waveforms using (a) conventional and (b) proposed modulation methods.



(a)



(b)

Fig. 6. Simulation results obtained for motor phase current using (a) conventional and (b) proposed modulation methods.

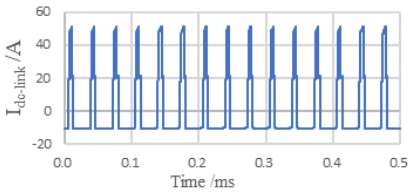
5. EXPERIMENT

The system shown in Fig. 1 was constructed for the experimental verification of the reduction effect of the $2f_c$ component of $I_{dc-link}$. The experiments were performed under the conditions listed in Table 3. To validate the accuracy of the simulations, the experimental results were compared with corresponding simulation results under the same conditions.

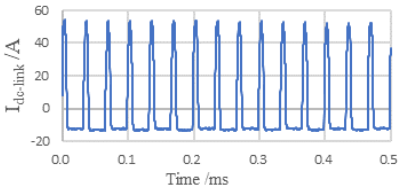
Table 3. Experimental conditions.

Name	Description	Value	Unit
fc	Carrier Frequency	15	kHz
Vdc	Inverter DC Voltage	50	V
Ia	Armature Current	37	A
cosθ	Power factor	0.99	-
M	Modulation Rate	0.22	-

Figures 7 and 8 show the time-domain and spectral waveforms of $I_{dc-link}$, respectively, under the conventional modulation method. These results indicate that the simulation reasonably represents the actual phenomena. Figures 9 and 10 show the time-domain and spectral waveforms of $I_{dc-link}$, respectively, under the proposed modulation. These results confirm that the simulation as well as experimental results indicated the same reduction effect of the $2f_c$ component of $I_{dc-link}$, demonstrating the usefulness of the proposed method.



(a)



(b)

Fig. 7. The (a) calculated and (b) measured $I_{dc-link}$ waveforms obtained using conventional method.

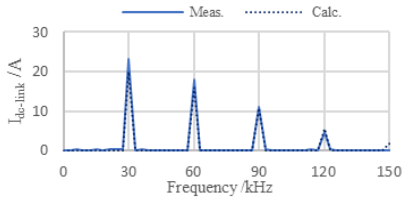
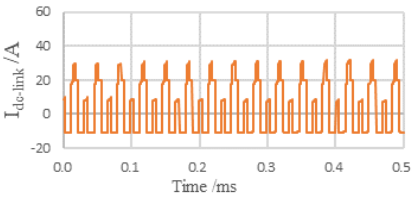
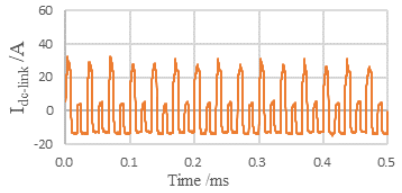


Fig. 8. Spectrum of $I_{dc-link}$ obtained using the conventional method.



(a)



(b)

Fig. 9. The (a) calculated and (b) measured $I_{dc-link}$ waveforms obtained using the proposed method.

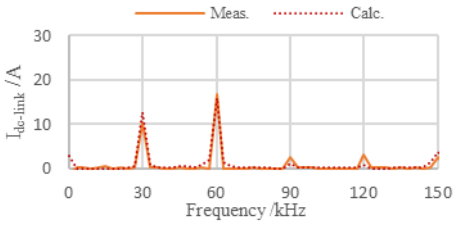


Fig. 10. $I_{dc-link}$ spectrum obtained using the proposed method.

6. CONCLUSION

This study proposes a modulation method to reduce the voltage ripple caused by DC-link capacitor used in a dual-inverter system for driving an open-end winding motor. Simulation results show that the proposed method can reduce the $2f_c$ component of $I_{dc-link}$, which is a major cause of DC-link voltage ripple. Furthermore, the experimental results validated the simulation results. The detailed impact of the proposed method on the motor current control and motor/inverter losses will be investigated in future studies.

REFERENCES

(1) C. S. Goli, S. Essakiappan, P. Sahu, M. Manjrekar and N. Shah, "Review of Recent Trends in Design of Traction Inverters for Electric Vehicle Applications," 2021 IEEE 12th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Chicago, IL, USA, 2021, pp. 1-6 .

(2) L. Chen and B. Ge, "High Power Traction Inverter Design and Comparison for Electric Vehicles," 2018 IEEE Transportation Electrification Conference and Expo (ITEC), Long Beach, CA, USA, 2018, pp. 583-588 .

(3) A. Safayet, M. Islam and T. Sebastian, "Sizing of DC-Link Capacitor Considering Voltage and Current Ripple Requirements for a 3-Phase Voltage Source Inverter," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2020, pp. 1512-1518 .

(4) B. P. McGrath and D. G. Holmes, "A General Analytical Method for Calculating Inverter DC-Link Current Harmonics," in IEEE Transactions on Industry Applications, vol. 45, no. 5, pp. 1851-1859, Sept.-oct. 2009 .

(5) K. Shibuya and N. Seki, “Zero-phase current reduction of open winding PMSM by phasor diagram applied zero-phase voltage determining method.,”*2021, IEE-Japan Industry Applications Society Conference,* 3-50, pp.III331-III334.

(6) S. Nakamura and K. Shibuya, “Zero-phase current reduction of open winding PMSM by phasor diagram applied zero-phase voltage determining method: 2nd report,” *2024, IEE-Japan Industry Applications Society Conference,* 3-38, pp.III259-III262.

(7) H. Zhan, Z. -q. Zhu and M. Odavic, "Analysis and Suppression of Zero Sequence Circulating Current in Open Winding PMSM Drives With Common DC Bus," in IEEE Transactions on Industry Applications, vol. 53, no. 4, pp. 3609-3620, July-Aug. 2017.