Finite Element Based Structural Validation of Printed Circuit Board Assemblies - Under Consideration of Static-, Vibrational- and Thermal Loads

Neubacher Christian, MSc [1)] Dr. Walter Hinterberger [2)]

1) MAGNA POWERTRAIN ENGINEERING CENTER STEYR GMBH & CO KG; Engineer Dynamics and Acoustics, Structural Analysis, St. Valentin, Austria

E-mail: Christian.Neubacher@magna.com

2) MAGNA POWERTRAIN ENGINEERING CENTER STEYR GMBH & CO KG; Lead Engineer Component Acoustics Analysis, Structural Analysis, St. Valentin, Austria

E-mail: Walter.Hinterberger@magna.com

ABSTRACT: This paper presents automated simulation processes, which can time efficiently predict chip crack zones, vibrational failure of solder-joints and thermal stresses of printed circuit board assemblies (PCBA). Application in an early design phase can save additional design loops as well as physical testing and therefore reduces development costs.

Each investigation starts by creating a finite-element model of the whole PCBA, using suitable discretization through automated modeling techniques based on ECAD data.

For static and dynamic investigations, the simulation effort can dramatically be reduced by material homogenization without a significant loss of accuracy. Inclusion of all surface mounted devices (SMDs) as well as the solder-joints, which are modelled using different sub-modelling and sub-structuring techniques complete the method. The resulting PCBA model is then used to calculate chip crack zones or its dynamic behavior for vibrational fatigue evaluation of each solder-joint.

For thermal investigations a fine discretized PCBA including all layers, traces and vias of the PCB has to be used. With sub-modelling techniques one can assess a detailed thermal stress analysis of critical regions (e.g. plated through holes – PTH) in the PCB. Examples for the structural reliability analysis of PCBAs are presented, and how these processes benefit from FEA process automation. Finally, comparisons between measurement and simulation are shown.

KEY WORDS: PCB, SMD, Solder-Joint, Automation, Finite-Element, Fatigue

1 INTRODUCTION

The trend towards electrification of vehicles requires an increased number of electronic components which need to withstand different environmental influences, like thermal, vibration and static loading. An essential part of the e-drive is the inverter, which includes printed circuit board assemblies (PCBA). These consist of the printed circuit boards (PCB) and different surface mounted devices (SMD), which are connected by solder-joints. The complexity of these systems makes it challenging to forecast potential failures.

However, it remains crucial to ensure that these systems can withstand the thermal, vibrational or static loads that occur during operation or even during the assembly process. Predicting possible damages in an early design phase by virtual testing can save additional design loops as well as physical testing and therefore reduces development costs. The following paper describes automated finite element-based modelling approaches and how these can be utilized in three different automated analysis processes:

- Vibration fatigue analysis of solder-joints
- PCB-strains analysis during assembly
- Thermo-mechanical analysis of stresses and strains

2 MODELLING APPROACHES

Modelling a PCBA can be split up into modelling of the PCB itself and modelling of the SMDs in conjunction with solder-joints.

2.1 PCB Modelling

The described modeling approaches are completely automated processes which transform ODB++ data into finite-element models. The ODB++ format is a standardized description of the E-CAD data, which contains for example the layers-information of the whole PCB (shape of traces, location of VIAs, etc…). [1]

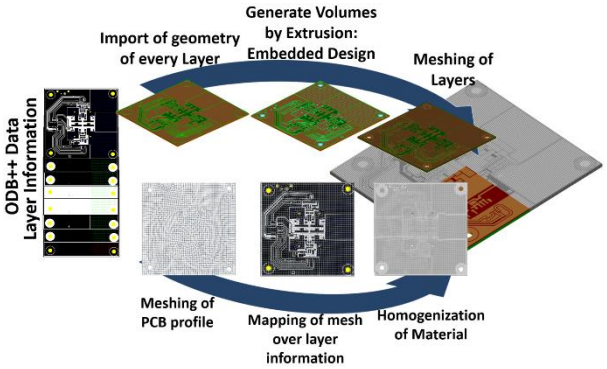

Fig. 1 PCB modelling approaches

2.1.1 Fine Modelling of the PCB

After reading the ODB++ data the automated process begins generating a 2D geometry of the profile for each layer of the PCB. In a further step all features of the PCB (traces, VIAs, holes, etc…) are projected onto the corresponding layers. An algorithm determines the necessary mesh size for different features of the PCB, making it finer in complex regions and coarser in simpler ones. The resulting 2D geometry of each layer is then meshed and extruded. Finally, the correct materials get assigned to the corresponding parts of the mesh.

The resulting finite element model contains all details of the PCB and is therefore typically large. When modelling bigger PCBs it is necessary to reduce the model size. This can be achieved by using a material homogenization process, see 2.1.2.

2.1.2 Material Homogenization

For most simulation use-cases it is necessary to reduce the model size while still maintaining the complex PCB characteristics. This is achieved by the material homogenization approach which uses the boundaries of every finite element from the PCB model to identify enclosed sections from the ODB++ data. Based on this enclosed geometry and material information one effective orthotropic material will be calculated for every element considering parallel and serial material combination in every dimension. This is achieved by using modified Reuss (isostress) or Voigt (isostrain) formulars [2].

2.2 SMD Modelling

A SMD database containing a simplified FE model (consisting of beams and shells) of each SMD package type and detailed solder-joint models (solid mesh) is used to reduce the modelling effort.

2.2.1 Device Modelling

If a new SMD package needs to be added to the database, its geometry data has to be specified according to the datasheet. An algorithm takes this data as an input and automatically generates a simplified SMD model with beam- and shell elements and adds it to the database for further use.

2.2.2 Solder-Joint Modelling

The shape of the solder-joint depends on the solder-type (see Fig. 2) and the size of the solder-pad. After specifying this data, the automated process utilizes a parametric CAD model as well as a parametric solder-joint FE-model of the corresponding solder-type. The solder-meniscus shape is automatically calculated taking physical parameters like surface tension during the soldering process and gravity into consideration [3]. The resulting geometry of the solder-meniscus is imported into the FE-preprocessor where it is automatically meshed and stored in a database similar to the simplified SMD model.

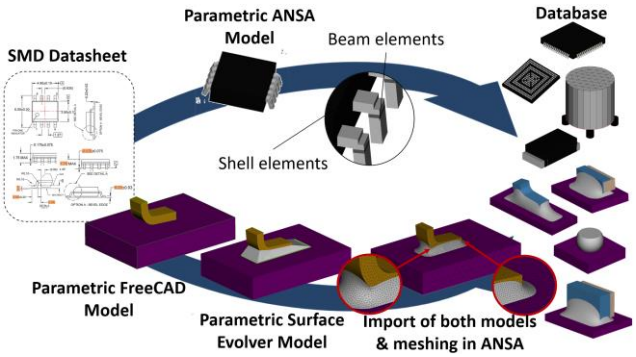

Fig. 2 Bottom: solder-joint sub models, top: simplified SMD models

3 SOLDER-JOINT FATIGUE

During operation of electric vehicles, the inverter PCBA has to endure different vibrational loads. These PCBAs can contain heavy components like transformators or electrolytic capacitors. As the solder-joints are often the only mechanical connection between the PCB and these heavy components they are especially susceptible to vibrational loads and therefore need to be evaluated [4].

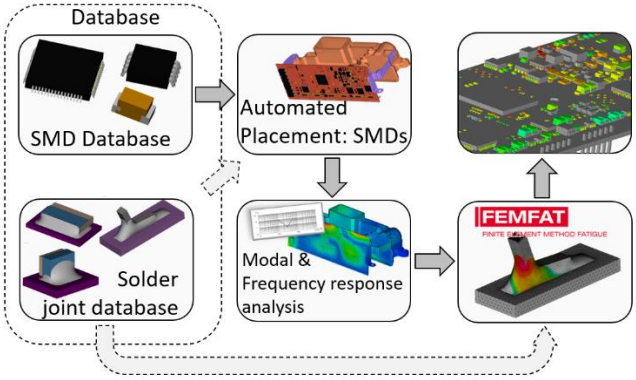

Fig. 3 Solder-Joint Fatigue calculation process

In a first step an overall PCBA model is automatically generated by placing the simplified SMD models onto the meshed PCB. The SMD pins representing the solder-joints are implemented as sub-structure. The resulting overall model is then used to conduct a modal reduced steady state dynamic analysis. In a subsequent FEMFAT analysis, the damage can be automatically assessed. This is achieved by mapping the frequency-dependent movement of each solder-joint pin onto the detailed sub-structure.

3.1 PCBA Finite Element Model

Due to the large number of SMDs on an inverter PCB (up to thousands) it is unfeasible to place all SMDs manually, thus the model generation needs to be automated. In the simulation process this is achieved by automatically placing the simplified finite element SMD models (via Pick&Place export) on a homogenized model of the PCB.

The beams of the simplified SMD models, representing the pins, are connected with ABAQUS substructure elements with two interface nodes taking the reduced stiffness matrix of the corresponding detailed solder-joint model into account (see Figure 2) [5].

3.2 Dynamic Simulation and Fatigue Assessment

A modal analysis followed by a frequency response analysis needs to be carried out for the overall model. The nodal displacements of both interface nodes from each substructure element are exported for every frequency and all degrees of freedom. Additionally for each new detailed solder-joint model in the database a static stress analysis with unit-displacements is conducted in all 6 degrees of freedom separately for both interface nodes of the sub-model. Both results together form the input for a solder-joint fatigue simulation.

Fatigue assessment: Stochastic load profiles like PSDs can be used as a direct input in FEMFAT Spectral. If a deterministic signal needs to be calculated (e.g. sine sweep or mechanical shock), the software tool Harmonic is used to generate the load-time history from the frequency response behavior, which is the input for a subsequent FEMFAT ChannelMAX analysis. The material data (ultimate strength, yield strength, S-N curve, etc…) for the FEMFAT analysis is based on literature like [6]. For each solder-joint an analysis job is automatically created and calculated. The maximum damage value of each solder-joint is mapped to one overall result file for further post processing. This allows a quick identification of critical areas on the PCBA.

Often, a shift of a critical SMDs to an other position is sufficient to mitigate the occurring damage. Furthermore, application of additional mounting points or adhesives on the PCB can reduce the overall mobility of the PCBA and therefore lower the solder-joint damage values. For more details see [7].

4 CHIP CRACK ANALYSIS

During the mounting process of a PCB into its housing the tolerances in the mounting points can lead to high strains in the PCB. This can cause problems for SMDs mode of brittle materials, especially for MLCCs (Multi Layer Ceramic Capacitors). Evaluating possible failures is essential to reduce defective products during production.

Due to the large number of mounting points in most assemblies' statistical approaches are necessary to calculate the critical tolerance cases. Two automated approaches were developed in order to evaluate the PCB strain:

- Worst case approach: This approach calculates the worst possible strain due to the given tolerances.
- Statistical: Calculates the strains based on the probability of occurrence

Press-fit connections to the PCB can lead to additional strains on the PCB during assembly. The maximum force of a press fit before it starts to slide can also be considered in both simulation variants.

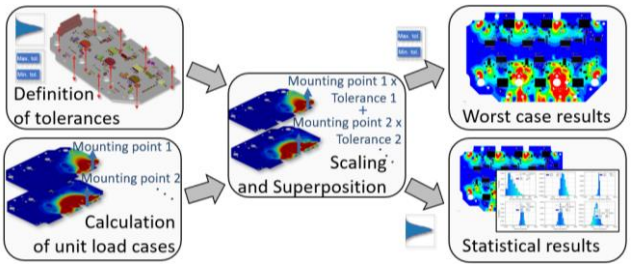

Fig. 4 Chip-Crack calculation Process

4.1 Finite Element Model

In this process a simple shell mesh of the PCB is generated. The inhomogeneous material distribution is considered by using the homogenization method described in chapter 2.1.2. The press-fit connections to the PCB are modelled via beam elements.

4.2 Calculation

The number of possible tolerance combinations depends on the number of mounting points. In the worst case approach every mounting point can be assigned either its maximum or minimum tolerance value. If a PCB has e.g. 15 mounting points this leads to $2^{15} = 32\,768$ possible tolerance combinations which are created automatically. In the statistical case there are an unlimited number of tolerance combinations. Every mounting point can be assigned a random variable out of a normal distribution. Usually about 15 000 tolerance cases are created automatically. The basis for the chip-crack calculation are the PCB strains due to unit displacement (ΔZ=1mm in normal PCB direction) of each mounting point. Since those strain/displacement transfer functions show linear elastic behavior, they can be scaled by the corresponding tolerance value. After scaling every transfer function, the final strain result of the PCB is generated by superposition. This process is repeated for every tolerance combination. In the worst case approach the maximum strain for every element out of every tolerance combination is displayed in one contour plot (see Fig. 4).

In the statistical case percentiles must be defined. The strain that doesn't get exceeded in the given percentile is then plotted in a contour plot.

Worst Case strain evaluation: $\max_{s \in S}\{\sum_{i=0}^{n} t_{n,s}\varepsilon_n^{PCB}\}$ (1)

Statistical strain evaluation: $P(\{\sum_{i=0}^{n} t_{n,s}\varepsilon_n^{PCB}\} \leq \varepsilon_p) \geq p$ (2)

where:

$$\varepsilon_n^{PCB} = f(\hat{u}_n)$$

ε^{PCB}… Strain unit displacement — $\hat{u}$… Unit displacement

t… tolerance sample — P… Probability

n… index of Mounting point — s… tolerance sample

ε_p… Percentile strain — p… Percentile

If a detailed evaluation for one finite element is needed the strain of all tolerance cases can be plotted in a histogram.

5 THERMO MECHANICAL ANALYSIS

During operation of an electric vehicle the inverter and its PCB must endure different thermal cycles. Due to the inhomogeneous composition of material with different thermal expansion properties these PCBAs can experience high stresses and strains even during homogeneous heat up.

5.1 Finite Element Model

In order to calculate the occurring stresses and strains due to the inhomogeneous material distribution a detailed FE model of the PCB containing all the layer information is necessary. In this case the fine-modelling approach in combination with the material homogenization approach can generate adequate models. The fine-modelling approach is used in areas where high stresses are suspected, and material homogenization is used for the remaining PCB to reduce the model size.

5.2 Calculation

Different thermal scenarios can be applied to the PCB model and a thermo-mechanical stress analysis can be conducted. Usually even during homogeneous heat up of the PCB (which occurs during every operation) leads to high internal stresses inside the PCB. VIAs and PTHs build a continuous plated-through copper connection between top and bottom layer of the PCB and can therefore experience high stresses in such cases. For these regions sub-models can be generated automatically which allow a detailed understanding of the occurring stresses.

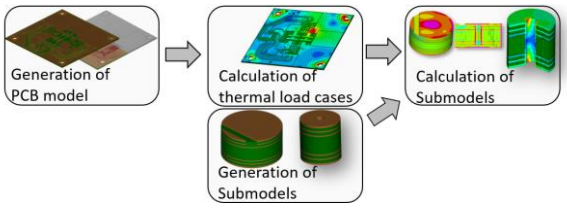

Fig. 5 Themo-mechanical calculation process

Usually adding thermal pads in critical regions or increasing the number of VIAs can lead to reduced stresses.

6 PROCESS VALIDATION

The processes described above were applied multiple times in e-drive projects and subsequently compared with measurement data. The accuracy of the simulation model is largely dependent on the used material data. Therefore, during development it was necessary to use measurement data to improve and adapt the described modelling and simulation processes for better correlation. The shown comparison between simulation and measurement represents the latest version of these improvements.

6.1 Solder-joint fatigue

Although the simulation processes aim to reduce the number of physical tests, it is still necessary to conduct measurements to validate the simulation results. During the e-drive development, the entire assembly is subjected to shaker tests. A vibration excitation is applied that traverses the simulated frequency range. Besides comparing the occurring damage, it is also possible to correlate the resonance frequencies of the PCB by measuring the overall PCB mobility during the vibration test with accelerometers or a laser vibrometer.

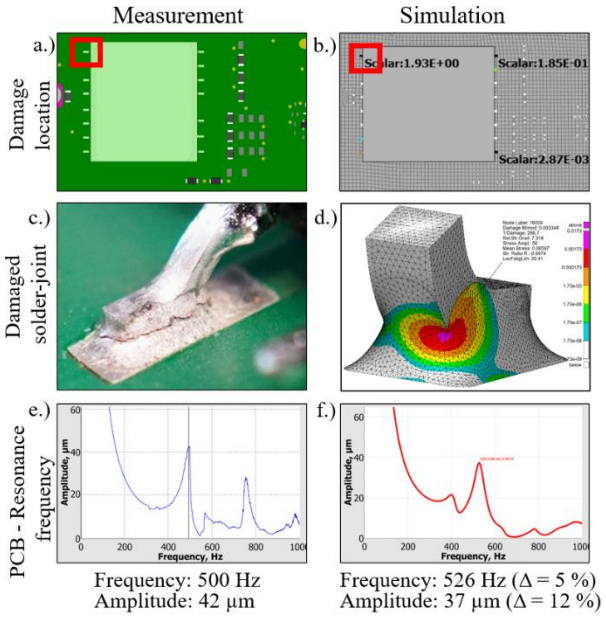

Fig. 6 Solder-joint fatigue comparison

In the example shown in Fig. 6 the correlation between the simulation and the vibration test measurement can be seen. In the simulation damage was predicted on the left upper pin (Fig. 6 b.) of the shown component. During testing a crack at this solder-joint (Fig. 6 a.) was observed. The simulation results (Fig. 6 d.) show that the initial crack starts at the meniscus of the solder-joint. The test results (Fig. 6 c.) show that this crack then extends all the way throughout the whole solder-joint. Additionally, the acceleration of the PCB at the solder-joint was measured in both cases. The frequency and amplitude of the first resonance was compared. In the simulation the resonance frequency was predicted at 526 Hz with an amplitude of 37 µm/m (Fig. 6 f.). During the test a frequency of 500 Hz with an amplitude of 42 µm/m was measured (Fig. 6 e.). This leads to a difference of 5% and 12% respectively. The deviation in frequency and amplitude can be caused by differences in overall stiffness and damping parameters in the system.

6.2 Chip-Crack analysis

In case of the Chip-Crack analysis a complete validation is a challenging task. This is because the results of this analysis are worst case strains or strains for different probabilities of occurrence due to the statistical distribution of the mounting point height tolerances. Nevertheless, usually tests are conducted where the PCB-strain during the assembly process is measured. Often the actual heights of PCB mounting points are additionally measured. In this case the tested tolerance sample can be simulated and directly compared. This is a meaningful comparison to validate modelling approaches, especially the homogenization (see 2.1.2), because the strains are strongly dependent on the material distribution inside the PCB which this approach aims to reflect. The example in Fig. 7 shows such comparison. In this case the strain on several points on the PCB were measured with strain gauges. The corresponding tolerance state then was simulated, and virtual strain gauges were applied on the same positions. The results of one strain gauge are compared in Fig. 7.

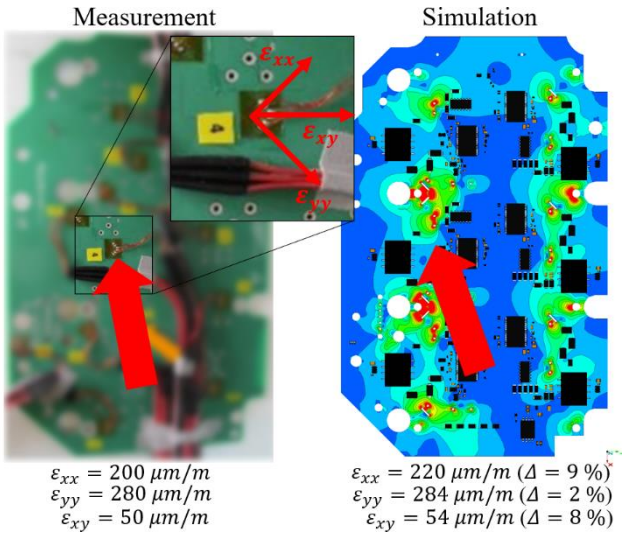

Fig. 7 Chip-Crack comparison

The used strain gauge was a rectangular 45° stacked rosette. The resulting 3 strain values $(\varepsilon_{xx}, \varepsilon_{yy}, \varepsilon_{xy})$ are evaluated in the local

coordinate system of the strain gauge. On the marked strain gauge in Fig. 7 the strain tensor was evaluated on the same position with the same orientation on the simulated PCB. Therefore, they can be directly compared. The simulation shows slightly higher strain values than the measurement. In the local x-direction the measured strain was 200 µm/m compared to 220 µm/m from the simulation. The best results can be seen in the local y-direction. Here the measured strain was 280 µm/m compared to 284 µm/m. The local shear strain component was 50 µm/m during testing compared to 54 µm/m. This leads to difference of 9%, 2% and 8% respectively. Overall, these differences are negligible, because there are still unknown factors that can influence the results, like the exact position of the strain gauge or manufacturing inaccuracies in the PCB, etc…

6.3 Thermo-mechanical

The following example shows a comparison between measurement and simulation for a thermo-mechanical problem. In both cases a PCB without SMDs inside an inverter was heated from 20°C up to 140°C and then cooled down to -40°C. The simulated PCB was modelled using the material homogenization approach (see 2.1.2). In the test setup the PCB - displacement was measured using a stereo-camera. The resulting displacement normal to the PCB of one point (marked by a red arrow in Fig. 8) is compared.

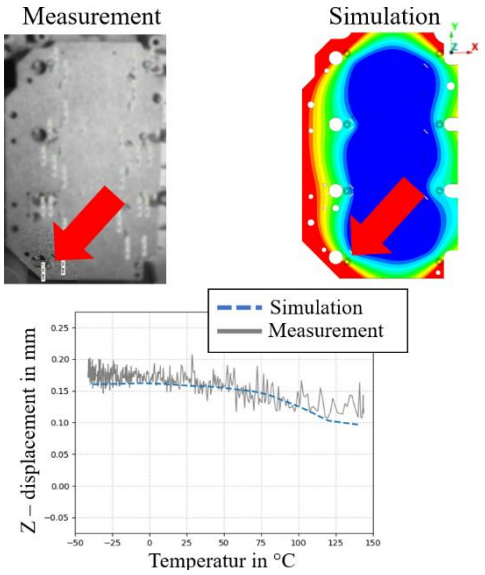

Fig. 8 Thermo-mechanical comparison

The diagram in the lower half of Fig. 8 shows the displacement of the evaluated point in the normal PCB direction over the temperature in comparison. As can be seen, both curves match very well. This indicates a good correlation between the measurement and the simulation. A slight offset in the simulation results is noticeable, which may suggest that the expansion coefficients are slightly too low. However, this offset is so small that it can be considered negligible.

7 CONCLUSION

Using automatization and different sub-structuring and sub-modelling techniques three processes were developed which time- and cost efficiently calculate the chip crack zones, failure of solder-joints and thermal stresses of printed circuit board assemblies (PCBA). Application of these simulation processes allows the identification of PCBA areas in an early design phase where improvements can prevent costly defects during later tests or even during operation. A validation between test data and simulation concludes this article, which demonstrates the accuracy of these techniques. All described methods are available in FEMFAT MELCOM software.

REFERENCES

[1] Siemens Digital Industries Software, „ODB++Design Format Specification Release 8.1 Update 4,“ August 2024. [Online]. Available: https://odbplusplus.com//wp-content/uploads/sites/2/2024/08/odb_spec_user.pdf. [Zugriff am 01 October 2024].

[2] M. Besenfelder MSc, FE-Modellierung und Analyse von Leiterplatten unter Berücksichtigung thermischer Lasten, Sieghartskirchen, 2021.

[3] K. A. Brakke, „The Surface Evolver,“ Experimental Mathematics, Bd. 1, Nr. 2, pp. 141-165, 1992.

[4] D. Steinberg, Vibration Analysis for Electronic Equipment, New York: John Wiley & Sons, Inc., 2000.

[5] Dassault Systemes, SIMULIA User Assistance 2020, Dassault Systemes, 2020.

[6] N. Barry, Lead-free Solders for High-Reliability Applications: High-Cycle Fatigue Studies, University of Birmingham, 2008.

[7] H. Ziegelwanger und W. Hinterberger, Fatigue analysis of solder-joints for vibration and shock, St. Valentin: MAGNA Powertrain, 2021.