A Capacitance Measurement Method for Power Modules in a Half-Bridge Topology for Automotive Applications

- A Simple Capacitance Measurement Method for Power Modules -

Jaewon Rhee [1], Sanguk Lee [1], Changmin Lee [1], Hyunsoo Lee [1], Hongseok Kim [1], Jiseong Kim [1], Seungyoung Ahn [1]

1) Korea Advanced Institute of Science and Technology, Cho Chun shik Graduate School of Mobility, Daejeon, Korea
E-mail: elly0386@kaist.ac.kr, sang960326@kaist.ac.kr, ckdals4707@kaist.ac.kr, hyunsoolee@kaist.ac.kr, kimhongseok@kaist.ac.kr, js.kim@kaist.ac.kr, sahn@kaist.ac.kr

ABSTRACT: This paper proposes a method for measuring the capacitance of power modules in inverters for vehicle motor drive applications. The capacitance of power modules can cause impedance changes in the current path, leading to switching noise. Therefore, an efficient measurement method is needed. Unlike the conventional multi-step measurement methods, a topology and a single-step measurement technique for extracting the capacitance of power modules is proposed. The capacitance between each terminal can be determined by performing S-parameter measurements on a 2-port network. The measured results are compared with datasheet values.

KEY WORDS: Capacitance, Half-bridge power module, S-parameter, Electromagnetic interference (EMI), Electric Vehicle.

1. INTRODUCTION

With the commercialization of electric vehicles, interest in power systems for driving motors has increased. Electric vehicles containing numerous electronic components are more susceptible to electromagnetic compatibility (EMC) and electromagnetic interference (EMI) issues compared to traditional power trains. Specifically, for motor operation within a vehicle, an inverter and a battery are essential, and the power semiconductors within the inverter can generate switching noise that affects other electronic components. The capacitance of power semiconductors alters the current path during switching on/off, which can induce high-frequency ringing noise. Thus, it is crucial to understand the switch capacitance that forms the power loop at the design stage. [(1)]

One of the significant challenges faced in these systems is EMI, which can degrade the performance and reliability of the power electronics. As electric vehicles require high-efficiency power conversion systems, the accurate measurement of capacitance is crucial for optimizing these systems. By understanding the behavior of parasitic capacitances, the design of power modules can be improved to reduce EMI, leading to better performance, efficiency, and safety in electric vehicles.

For the miniaturization and weight reduction of automotive electronic components, module-based integration is becoming common. Switches in inverters are also increasingly manufactured as modules with half-bridge topologies instead of individual switches. Therefore, it is essential to measure the capacitance at the module level, including the package, necessitating a unique capacitance measurement method. [(2)]

While numerous studies have focused on extracting parasitic components of individual switches, they are not suitable for application in power modules. In individual switches, an impedance analyzer can be used to perform a 1-port measurement by floating one of the terminals of MOSFET. However, this approach reduces measurement accuracy due to parasitic capacitance between the floating port and the ground. [(3)] Subsequent studies connected the gate to the ground and measured the parasitic components using a 2-port approach with the drain and source. [(3-4)] However, to measure all ports of a MOSFET in a half-bridge configuration without floating any terminals, these studies required a 5-step process, changing terminal connections for each step. This requires multiple measurement steps and five fixtures, presenting limitations. [(5)]

In this study, we propose a method for measuring the capacitance of a half-bridge module in a single measurement, without floating errors. All MOSFET ports are connected or grounded to eliminate floating errors. Furthermore, without changing terminal connections or using multiple fixtures, we

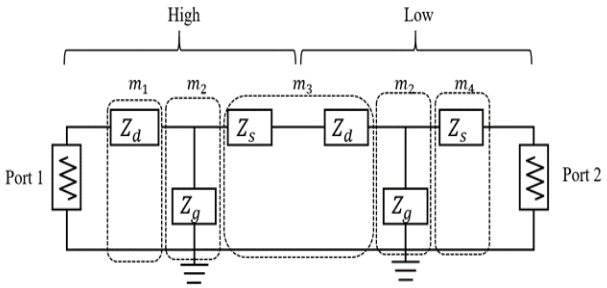

Fig. 1 Proposed Topology for Capacitance Measurement.

developed a method that extracts the capacitance with a single measurement.

2. Capacitance Extraction Method

To address the limitations of existing methods, this study proposes a method to extract the parasitic capacitance of a half-bridge MOSFET with a single 2-port S-parameter measurement. All terminals are connected without floating, and a 2-port network-based extraction method is proposed.

Existing methods, such as those using traditional network analyzers, often struggle with accuracy in multi-port power modules due to complex parasitic elements that are difficult to measure in real-time. Moreover, these methods require substantial post-processing of data to accurately calculate capacitance, which makes them inefficient for practical applications. In contrast, the proposed method provides a real-time, highly accurate capacitance extraction model based on impedance measurements. By using a frequency-domain approach, it minimizes the need for extensive data processing and delivers results that can be directly applied to design and optimization processes.

Fig. 1 shows the equivalent circuit for extracting parasitic components of a half-bridge MOSFET. Z_{g}, Z_{d}, and Z_{s} are the impedances of the gate, drain, and source terminals, respectively. Both high-side and low-side gate (Z_{g}) terminals are connected to the ground, while ports are connected to the high-drain (Z_d) and low-source (Z_s). The equivalent circuit is composed of two connected star circuits, and the extraction method utilizes 2-port network theory to represent it in terms of ABCD parameters. Equations (1) – (5) describe the process of deriving the ABCD parameter based on Fig. 1.

$$M = m_1 m_2 m_3 m_2 m_4 = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \tag{1}$$

$$A = \frac{Z_d^2 + Z_g^2 + 3Z_d Z_g + Z_s Z_d + Z_s Z_g}{Z_g^2} \tag{2}$$

$$B = \frac{Z_d^2(Z_g + Z_s) + 2Z_g^2(Z_d + Z_s) + Z_s^2(Z_g + Z_d) + 4(Z_d Z_g Z_s)}{Z_g^2} \tag{3}$$

$$C = \frac{Z_d + 2Z_g + Z_s}{Z_g^2} \tag{4}$$

$$D = \frac{Z_g^2 + Z_s^2 + 3Z_s Z_g + Z_g Z_d + Z_s Z_d}{Z_g^2} \tag{5}$$

The ABCD parameters of the proposed topology can be converted to Z parameters, as shown in equations (6) – (9).

$$Z = \frac{1}{C}\begin{bmatrix} A & |AD - BC| \\ 1 & D \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \tag{6}$$

$$Z_{11} = \frac{Z_d^2 + Z_g^2 + 3Z_d Z_g + Z_s Z_d + Z_s Z_g}{Z_d + 2Z_g + Z_s} \tag{7}$$

$$Z_{12} = Z_{21} = \frac{Z_g^2}{Z_d + 2Z_g + Z_s} \tag{8}$$

$$Z_{22} = \frac{Z_s^2 + Z_g^2 + 3Z_s Z_g + Z_g Z_d + Z_s Z_d}{Z_d + 2Z_g + Z_s} \tag{9}$$

By solving the resulting three simultaneous equations from equations (7) – (9), the impedances of the gate, drain, and source can be obtained, as shown in equations (10) – (12).

$$Z_g = \sqrt{Z_{21}(Z_{11} + 2Z_{21} + Z_{22})} \tag{10}$$

$$Z_d = Z_{11} + Z_{21} - Z_g \tag{11}$$

$$Z_s = Z_{22} + Z_{21} - Z_g \tag{12}$$

Ultimately, by converting the measured S-parameters to Z-parameters, the impedance of each terminal can be determined with a single measurement.

3. Experiment Verification

To validate the proposed method, we selected a commercial half-bridge module from Infineon (IAUC60N04S6N031H), designed a test fixture, and conducted measurements. Fig. 2 shows the measurement setup, with a vector network analyzer (VNA) used for 2-port S-parameter measurements. Gate pins were connected to the ground using vias to ground the gates of each MOSFET. The measurement frequency was set to 1 MHz, which is consistent with the datasheet. The measured S-parameters were converted to Z-parameters and calculated using equations (10) – (12).

The measurement results are shown in Table 1, where the value of $\mathrm{C_{dg}}$ shows a maximum deviation of 8.8% compared to the datasheet. The smaller capacitance value of $\mathrm{C_{dg}}$ proves challenging to measure, confirming the effectiveness of the proposed method for capacitance extraction.

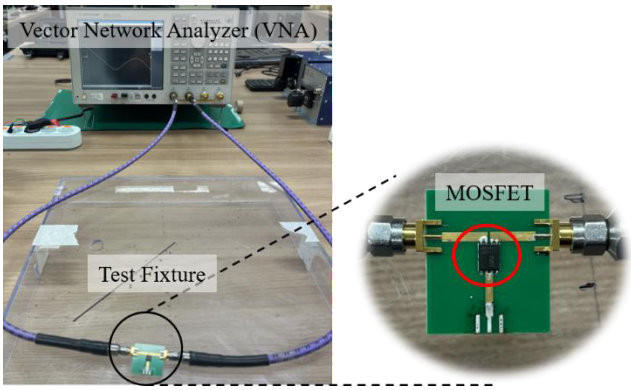

Fig. 2 Experimental Setup for Capacitance Measurement.

Table 1 Comparison of Measurement Results with Datasheet.

	C_{ds} [pF]	C_{dg} [pF]	C_{gs} [pF]
Datasheet [pF]	1850	274.9	1420
Measurement [pF]	1853	277	1424
Difference	0.16%	0.76%	0.28%

The experiments were conducted using a network analyzer to measure the impedance of the power module across a wide frequency range. The results from the proposed capacitance extraction method were compared to those obtained from traditional measurement techniques, such as curve tracers, to assess its accuracy and efficiency. Additionally, the impact of measurement errors on capacitance extraction was carefully analyzed by performing measurements. These experiments demonstrated that the proposed method consistently delivered more accurate and reliable capacitance values.

The measurement results were also compared with the capacitance extracted from the SPICE model in Fig.3 provided by the vendor. The comparison was conducted with the SPICE level 1 (Infineon's own standard) model provided by Infineon, and the capacitance of each terminal was extracted using the Advanced Design System (ADS).

C_{gs}, which has little change depending on the DC voltage, is modeled as a constant of 1420 pF, and C_{dg} and C_{ds} are modeled as diodes to model the change depending on the voltage [6]. Since the junction capacitance of the diode is the capacitance when the DC voltage is 0 V, the capacitance extracted from the SPICE model is shown in Table 2.

There are some differences from the data sheet results provided by the vendor, and this may be a value selected to simplify the

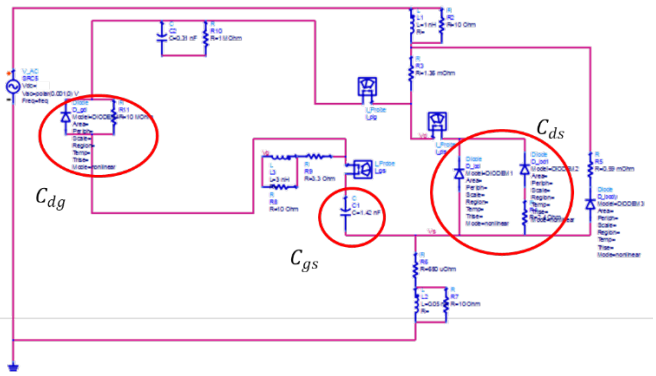

Fig. 3 Vendor SPICE model (IAUC60N04S6N031H).

Table 2 Comparison of Measurement Results with SPICE model.

	C_{ds} [pF]	C_{dg} [pF]	C_{gs} [pF]
SPICE [pF]	2620	310	1420
Measurement [pF]	1853	277	1424
Difference	29.27%	10.65%	0.28%

SPICE model. The SPICE model needs to be updated based on the measurement results in the future.

4. CONCLUSIONS

This paper proposes a method for easily extracting parasitic components in half-bridge power modules, which are increasingly used due to the miniaturization of MOSFETs. Parasitic capacitance in MOSFETs can induce oscillations and overshoot, leading to switching noise. Therefore, accurately extracting parasitic capacitance is essential, and it requires connecting or grounding all terminals without floating errors. Unlike single MOSFET, where increased terminals make it necessary to change terminal connections, this method allows for capacitance extraction of half-bridge MOSFETs through a single measurement. The effectiveness of this method was validated through measurements. The proposed capacitance extraction method not only improves the efficiency of capacitance measurement process but also lays the groundwork for future developments in real-time EMI mitigation strategies. By enabling more accurate and efficient measurement of parasitic capacitances, this method can significantly contribute to the design of next-generation power electronics used in electric vehicles and renewable energy systems. Furthermore, future work will focus on extending this method to more complex multi-chip power modules and incorporating it into automated design tools for power electronics optimization.

ACKNOWLEDGMENT

This work was supported by the Institute of Information & communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (MSIT) (No.2020-0-00839, Development of Advanced Power and Signal EMC Technologies for Hyper-connected E-Vehicle).

REFERENCES

(1) K. Wang, H. Lu, C. Chen and Y. Xiong, "Modeling of System-Level Conducted EMI of the High-Voltage Electric Drive System in Electric Vehicles," *IEEE Transactions on Electromagnetic Compatibility*, vol. 64, no. 3, pp. 741-749, June 2022.

(2) D. N. Dalal et al., "Impact of Power Module Parasitic Capacitances on Medium-Voltage SiC MOSFETs Switching Transients," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 298-310, March 2020.

(3) A. N. Lemmon and R. C. Graves, "Comprehensive Characterization of 10-kV Silicon Carbide Half-Bridge Modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 4, pp. 1462-1473, Dec. 2016.

(4) T. Liu, T. T. Y. Wong, and Z. J. Shen, "A New Characterization Technique for Extracting Parasitic Inductances of SiC Power MOSFETs in Discrete and Module Packages Based on Two-Port S-Parameters Measurement," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9819-9833, Nov. 2018.

(5) R. Zhong et al., "A Simplified Method for Extracting Parasitic Inductances of MOSFET-Based Half-Bridge Circuit," *IEEE Access*, vol. 9, pp. 14122-14129, 2021.

(6) J. Rhee, S. Lee, H. Kim, J. Kim, and S. Ahn, "A Simple Characterization Method for Parasitic Capacitances Extraction of SiC Power MOSFETs Integrated Half-bridge Configuration," *IEEE Journal of Emerging and Selected Topics in Power Electronics* (Early access).